Remarks

Claims 1 - 9 are pending. Favorable reconsideration is respectfully requested.

There is an apparent error in the Office Action dated April 14, which states that claims 5 - 9 are withdrawn from consideration "[b]ecause applicant did not distinctly point out the supposed errors in the restriction requirement . . . ." This is incorrect, and claims 5 - 9 have never been restricted. In the Restriction Requirement of September 29, 2005, a restriction was imposed between Group I, claims 1 - 3 and 5 - 9, and Group II, claim 4. Applicants elected the Group I claims with traverse, i.e. claims 1- 3 and 5 - 9, giving reasons therefore on pages 1 and 2 of their response dated October 13, 2005.

In the Election of Species requirement of January 6, 2006 the Examiner required Applicants to elect the species of claims 1 - 3 or the species of claims 5 - 9 for initial examination. Applicants elected the species of claims 1 - 3. An election of species requirement is not a restriction requirement, and per the MPEP, should the examined species be found patentable, examination of a limited number of additional species must follow. In this case, claim 1 is generic, because all of claims 2, 3, and 5 - 9 are dependent upon claim 1, and include all of its limitations. If claim 1 is found patentable, then the remaining claims must be patentable as well. Claim 1 is a generic claim.

With respect to claim 4, the burden is upon the Office to produce evidence refuting Applicants' traversal of the restriction requirement. Applicants' traversal provided good and sufficient reasons why the proposed restriction was improper. In view of this response, the burden shifts back to the Office to provide additional evidence supporting the right of the Office to restrict the claims. The Office simply removed claim 4 from consideration without comment. This action is procedurally and legally inadequate. The Commissioner himself has recently deplored the number of divisional and continuation applications being filed, stating that these applications place an enormous burden on the Office.

Reinstatement of claim 4 or the providing of evidence in support of the withdrawal of claim 4 is solicited.

Claims 1 - 3 have been rejected under 35 U.S.C. § 102(b) over Wenski U.S. Patent 6,548,688 ("*Wenski*"), commonly assigned. Applicants respectfully traverse this rejection.

The subject application is directed to a process for producing a semiconductor wafer which has exceptional suitability for the preparation of circuitry to 0.1 μm design rules, and to the wafer thus produced. The process produces a wafer having a back side with an edge region which, from a radial distance 6 mm to 1 mm from the wafer edge deviates from the plane of the wafer back side by no more than 0.7 μm. While circuits are fabricated on the wafer front side, it has been found that back side deviations from planarity have a large influence on the ability to successfully implement such circuitry, particularly the back side wafer periphery geometry.

The claims have been rejected under 35 U.S.C. § 102(b) over Wenski et al. U.S. 6,458,688. The Office states that:

> Wenski et al. discloses a polished semiconductor wafer with a front surface, a back surface and a peripheral are [sic] of the semiconductor wafer having a flatness values of less than or equal to 0.13 micron which is within the claimed range of 0.5 micron or less (see figs. 1 - 4 and related text).

However, it is noted that the flatness values referred to in the claims, are the flatness of a peripheral region, which lies in a narrow circumferential zone beginning 1 mm from the wafer edge and extending to 6 mm from the wafer edge. Moreover, it is noted, importantly, that this peripheral region is on the back side, not the front side, of the wafer.

Wenski does not disclose any backside geometry. Rather, he measures only the front surface topology. *See, e.g.* column 2, lines 48 - 50:

> and flatness values based on partial areas of a surface grid on the front surface of the semiconductor wafer.

Wenski does not disclose any back side measurements. Moreover, even *Wenski's* frontside measurements are made on a grid with a 3 mm edge exclusion. *See, e.g.* column 8, lines 53 - 56:

> local geometry SPQR (grid 25 mm x 25 mm) were measured on a commercially available geometry gauge with 3 mm edge exclusion. (emphasis added).

Thus, the geometry of the R-1 to R-3 area, the portion of the wafer with the greatest deviation from flatness (except the R to R-1mm chamfered edge itself) is not even included in the measurement.

It is well known to those skilled in the skilled in the art that the front side and back side wafer topographies achieved during double sided polishing are very different. The distribution of polishing slurry and temperature differences alone dictate that this is an inherent and unavoidable result. In addition, sedimentation of both abrasive and abraded particles due to gravity is different with respect to particle size of the polishing slurry abrasive, and thus the polishing slurry "seen" by the bottom of the wafer is different from that seen by the front surface, and produces a different surface.

Wenski does not disclose, nor does he search or suggest any wafer or process for producing a wafer, wherein the periphery ranging from 1 to 6 mm from the edge of the back side of the wafer deviates no more than 0.7 μm from the plane of the wafer; neither do any of the other references cited but not used in rejecting the claims.

Nor can the rejection be based on inherency. In rejections based on inherency, the inherency must be certain, *Ex parte McQueen*, 123 USPQ 37 (POBA 1958), *Ex parte Cyba*, 155 USPQ 756 (POBA 1966); and must be a necessary result, and not merely a possible result. *Ex parte Keith*, 154 USPQ 320 (POBA 1966). Recent Federal Circuit cases have re-echoed these principles, requiring that missing descriptive material be "necessarily present" and not merely "probably" or "possibly" present, *In re Robertson*, 49 USPQ2d 1949 (Fed. Cir. 1999), and must meet a "strict identity test" for anticipation. *Trintec Industries, Inc. v. Top-U.S.A. Corporation*, 63 USPQ2d 1597 (Fed. Cir. 2002).

Here, there is absolutely no reason why the *Wenski* wafer backside edge periphery topology should be within 0.7 μm of the wafer plane. Applicants' claimed result is not only not a necessary condition, it is not even a probable condition. Withdrawal of the rejections of claims 1 - 3 and 5 - 9 is solicited.

Respectfully submitted,

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